Simulink Model of a 3-Level Voltage Fed Soft-Switching Inverter with Two ARDCL Snubbers

Ali Kadhim Abdul-Abbas , Rabee' Hashim Thejel , Haroutuon A. Hairik

***Abstract*—This paper presents a new simulation soft switching three level inverter using MATLAB program. This circuit uses two identical Auxiliary Active Resonant DC Link (ARDCL) snubbers connected to the high voltage DC bus line of three-level inverter. The circuit has the flexibility of selecting switching instants of the resonant link in synchronism with SVPWM technique. Control technique does not require the help of inverter switches to create the zero voltage instants in the main switches. In this paper, the principle of operation and detailed analysis of the proposed ARDCL inverter are presented and design considerations for achieving soft switching are obtained. Detailed MATLAB simulation studies are carried out to study the feasibility of the proposed topology under various load condition.**

key word: multilevel inverter, soft switching, Matlab/simulation

I. INTRODUCTION

Multilevel inverters are being increasingly used in high power industrial application due to their compatibility for medium voltage and improved output performance at that voltage as compared to two-level inverter [1,2,3].

Among various modulation techniques for a multilevel inverter, Space Vector Pulse Width Modulation (SVPWM) is an attractive candidate due to the following merits: It directly uses the control variable given by the control system and identifies each switching vector as a point in complex (α, β) space, it is useful in improving DC link voltage utilization, reducing commutation losses and THD [4,5].

In recent years, soft switching power conversion circuit and system technologies have attracted special interest as next generation power converters, which can achieve efficiency improvement in high-frequency switching and lowered electromagnetic noises [6,7]. In general, soft switching power conversion circuit topologies can be classified into four types: resonant DC link snubber, resonant AC link snubber, auxiliary resonant commutated snubber and resonant switching block link snubber[8].

This paper presents the operation performance of modified type of Auxiliary Resonant DC Link snubber inverter, The operation principle of this circuit and operation modes of space vector three level inverter which incorporates soft switching circuit is described on the basis on performance evaluation which includes simplified implementation, reduced auxiliary power semiconductor device and circuit component stresses.

This soft switching compared with the conventional three-phase three-level hard switching inverter under the conditions of specified parameters. Theoretical study and computer simulation using MATLAB/Simulink program are presented.

II. SVPWM DIODE-CLAMP THERR LEVEL THREE PHASE VOLTAGE SOURCE INVERTER

The three level converters, also known as a (neutral-clamped) converter, consist of two capacitor voltages in series and use the center tap as the neutral. The circuit of three-phase three-level voltage source inverter is shown in Fig.1.

A. Analysis of Operation Modes

Mode-A (mode_1)**:**

When switches S_{1a} , S_{1b} are ON and S_{4a} , S_{4b} are OFF , then the output voltage is $+V_{dc}/2$ for positive phase current ($i_a > 0$). On the other hand switches (diodes) D_{1a} and D_{1b} are ON when ($i_a < 0$).

Mode-B (mode_0)

State-B of inverter operation is gained when switches S_{1b} and S_{4a} are ON and S_{1a} and S_{4b} are OFF. Switch S_{1b} is conducting for $i_a > 0$ and S_{4a} for $i_a < 0$.

Mode-C (mode_-1)

State-C of inverter operation is gained when switches S_{4a} and S_{4b} are ON and S_{1a} and S_b are OFF. Switches (diodes) D_{4a} and D_{4b} are ON when $i_a > 0$ and switches S_{4a} and S_{4b} are ON when $i_a < 0$.

B. Theory and Operation of SVPWM

Space vector modulation is based on transforming three phase quantities into the α-β plane. In general, a three phase n-level VSI has a total of n^3 space vectors, thus in the case of three-phase three level VSI there are 27 space vectors that represent the different combinations of the ON/OFF of the twelve switches of the three-phase VSI[9]

The space vector of phase voltage $\overline{V}_{\alpha\beta}$ can be defined in αβ-reference frame as follows

$$\overline{V}_{\alpha\beta} = \frac{2}{3}[\overline{V}_a + \bar{a}\overline{V}_b + \bar{a}^2\overline{V}_c] \qquad \ldots\ldots\ldots (1)$$

where $a=e^{j(2/3)\pi}$ is the complex operator and $\overline{V}_a$, $\overline{V}_b$ and $\overline{V}_c$ are voltages of terminals A, B and C with respect to the neutral point O of DC bus.

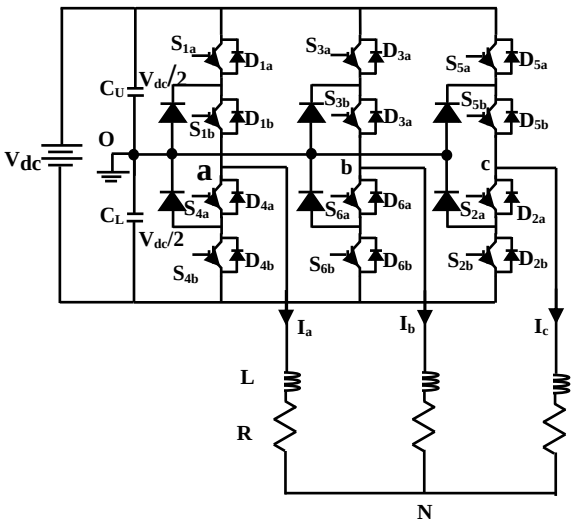

Fig.1 Three phase three-level diode-clamping VSI.

The magnitudes of the space vectors shown in Fig.2 have only four values as follows:

(i) Large magnitude with 2/3 p.u. value .
(ii) Medium magnitude with 1/√3 p.u. value.
(iii) Small magnitude with 1/3 p.u. value.
(iv) Zero magnitude.

The angle between adjacent space vectors is 30º which divide the space vector diagram into 12 sectors (from sector I to sector XII) and three planes.

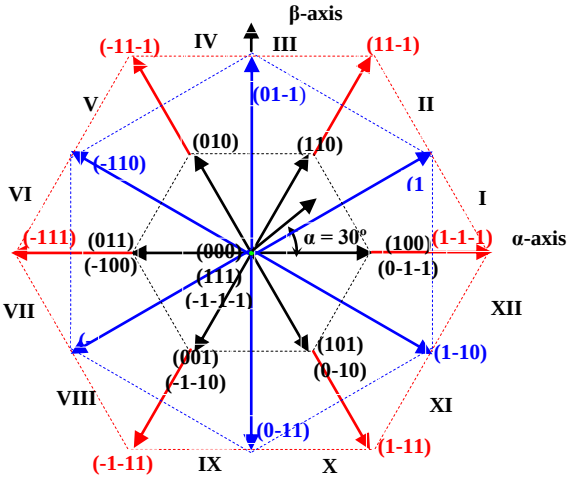

Fig.2 Three-phase VSI phase voltage space vectors in the αβ plane.

C. Generation of The Inverter Switching Sequence

The basic idea of space vector modulation is to compensate the required volt-seconds using discrete switching states and their on-times produced by inverter [10]. Based on the principle of volt-second equivalent, that is volt-second value balance between magnitude of the reference vector and the actual switching state vectors, conventional space vector modulator uses the nearest three vectors (small, medium and large) and zero vector in one sector to approximate reference voltage vector. Three main issues should be solved in SVPWM procedure: detection of nearest three voltage vectors to the reference vector, determining of the corresponding function time and the processing sequence of those three voltage vectors.

In order to detect the nearest three vectors to the reference vector, the traditional SVPWM method compares the reference vector with all the divided sections in turn under α-β reference frame. The computation is relative complex in a three-level converter.

In this work, one large, medium and small space vectors are utilized to generate the required gating pulses for the αβ-plane of the three-phase inverter.

The times (t_a and t_b) can be calculated using large and medium space vectors, then for odd-numbered sectors

$$t_a = \frac{V_s^* t_s \sin(k\frac{\pi}{6} - \alpha_s)}{V_l \sin(\frac{\pi}{6})}$$

$$t_b = \frac{V_s^* t_s \sin[\alpha_s - (k-1)\frac{\pi}{6}]}{V_m \sin(\frac{\pi}{6})} \quad \text{…….. (2)}$$

And for even-numbered sectors

$$t_a = \frac{V_s^* t_s \sin(k\frac{\pi}{6} - \alpha_s)}{V_m \sin(\frac{\pi}{6})}$$

$$t_b = \frac{V_s^* t_s \sin[\alpha_s - (k-1)\frac{\pi}{6}]}{V_l \sin(\frac{\pi}{6})} \quad \text{…….. (3)}$$

The application times of large, medium and small space vectors can be calculated as follows

$$t_{as} = \frac{t_a V_{sm}}{V_l + V_m + V_{sm}}$$

$$t_{am} = \frac{t_a V_m}{V_l + V_m + V_{sm}}$$

$$t_{al} = \frac{t_a V_l}{V_l + V_m + V_{sm}} \quad \text{……. (4)}$$

$$t_{bs} = \frac{t_b V_{sm}}{V_l + V_m + V_{sm}}$$

$$t_{bm} = \frac{t_b V_m}{V_l + V_m + V_{sm}}$$

$$t_b = \frac{t_a V_l}{V_l + V_m + V_{sm}}$$

The switching patterns of the space vectors that utilize small, medium and large neighboring space vectors for sectors I and II can be shown in Figs. 3 and 4.

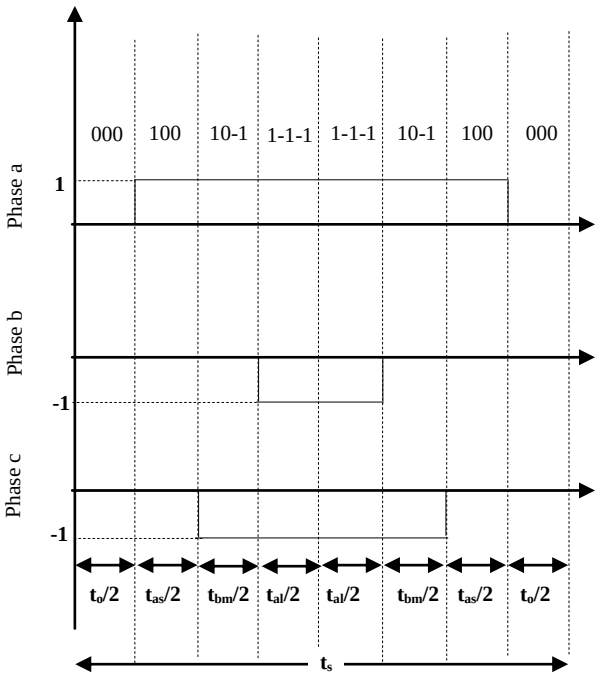

Fig.3 Switching pattern (sector I) with utilizing small, medium and large neighboring space vectors.

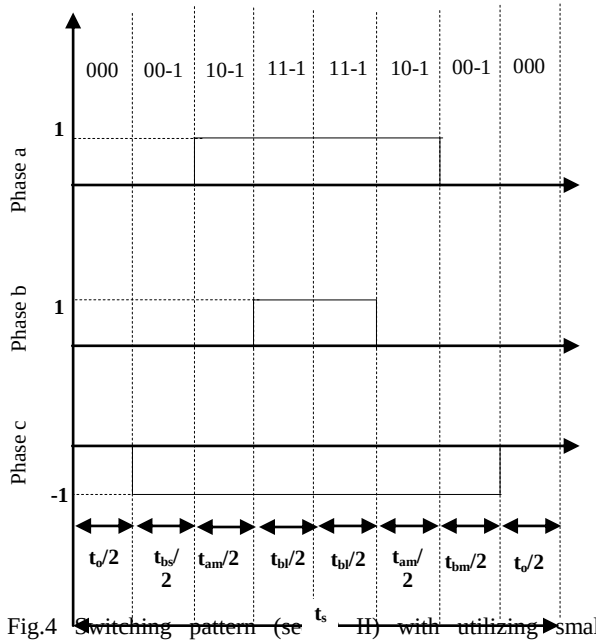

Fig.4 Switching pattern (se II) with utilizing small, medium and large neighboring space vectors.

The time t_o can be calculated for any sector using these figures. For odd-numbered sectors it is:

$$t_o = t_s \quad (t_{al} + t_{bm} + t_{as}) \qquad \ldots\ldots\ldots (5)$$

And for even-numbered sectors:

$$t_o = t_s - (t_{bl} + t_{am} + t_{bs}) \qquad \ldots\ldots\ldots (6)$$

where t_o is time of application of zero space vector.

D. Software Simulation of Space Vector Pulse Width Modulation

The Simulink model for generating of the inverter switching pulses in the αβ-plane is implemented using Eqs.(2)-(6) with the aid of the switching pattern of the twelve sectors and a sector indicator facility. This model is shown in Fig.5. In this figure: F(u)1 and F(u)2 blocks are used to determine the sector number (K) through calculation of α_s from frequency (f_1). F(u)3 and F(u)4 blocks are used to calculate t_a and t_b according to Eqs. (3) and (4). F(u)5 to F(u)10 blocks are used to calculate t_{al} , t_{am} , t_{as} , t_{bl} , t_{bm} , t_{bs} according to Eq. (4). f_1 is frequency of the output voltage in αβ-plane. f_s= 10 kHz =Switching frequency. V_s^* is the reference space vector voltage for the three-phase load.

Output of F(u)5 to F(u)10 blocks , sector number (K) , time of sample (t_s) and time (t) are input to crossing block which is a Matlab M-file software program. M-file generates the 3-phase VSI switching pulses according to the switching pattern of the twelve sectors.

E. Simulation Result

In this section, simulation is performed for the proposed space vector pulse width modulation by using Matlab/Simulink program. Figs. 6-8 show voltage and current for modulation index 0.85 and harmonic spectrum is shown in Fig. 9.

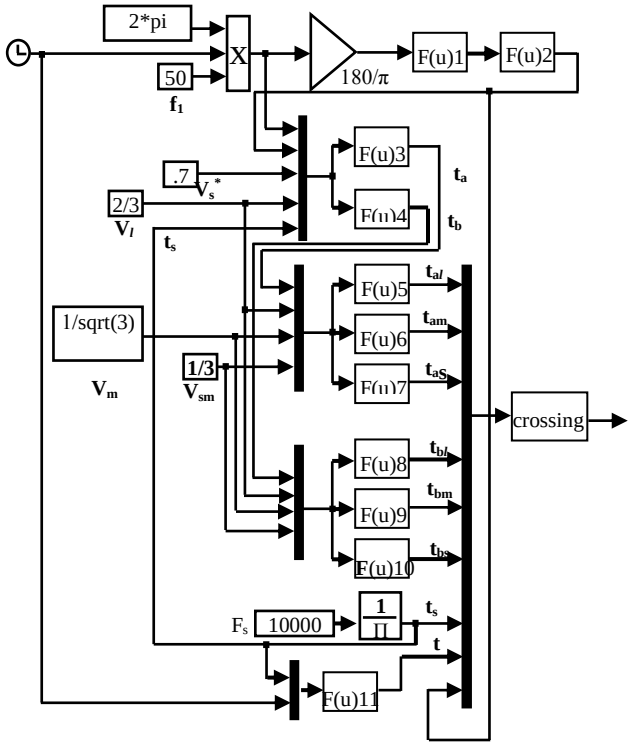

Fig.5 Implemented simulink model for the generation of three-phase inverter pulses.

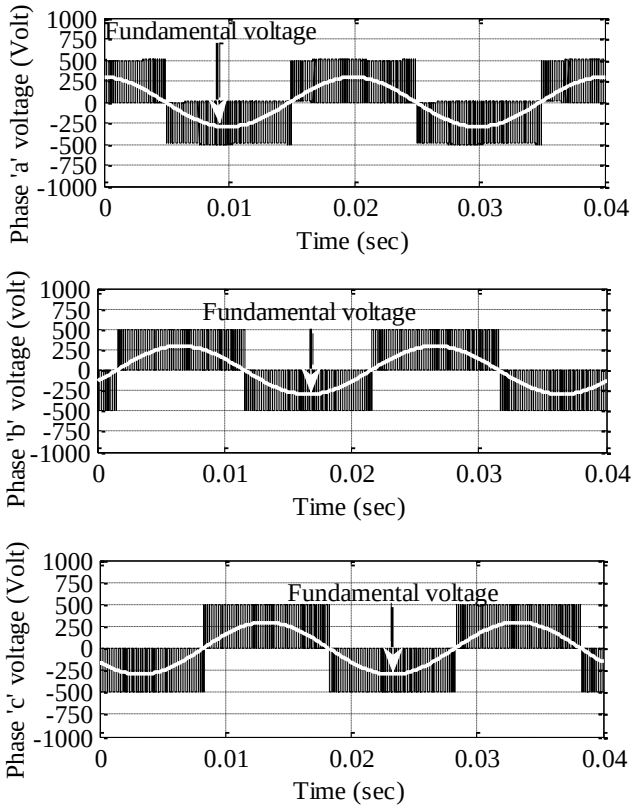

Fig.6 Inverter phase voltages for a reference voltage of 0.85 pu.

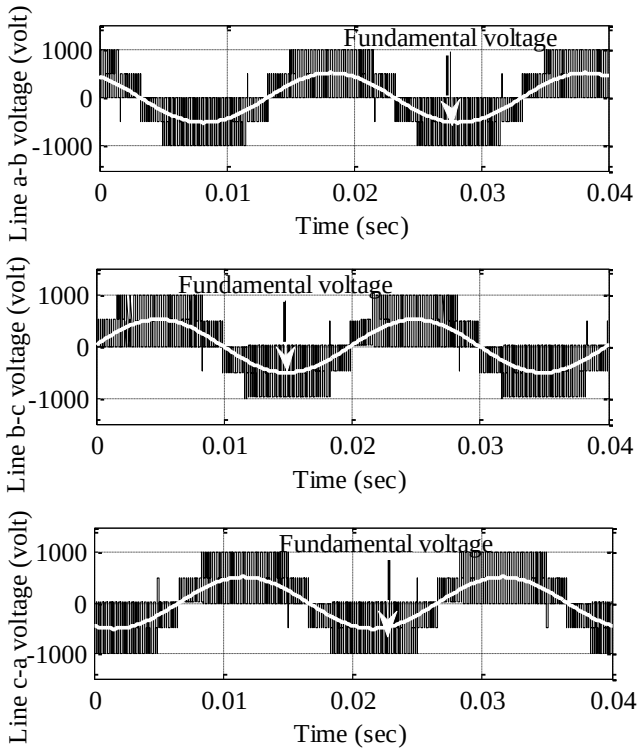

Fig.7 Inverter line voltages for a reference voltage of 0.85 pu.

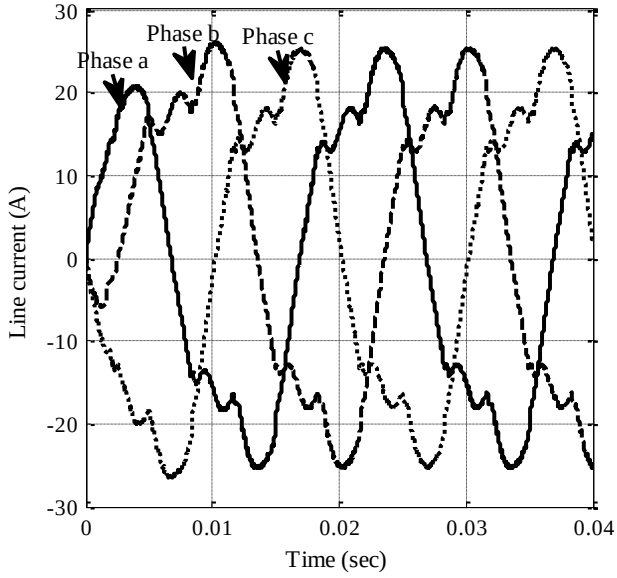

Fig.8 Inverter line currents for a reference voltage of 0.85 pu.

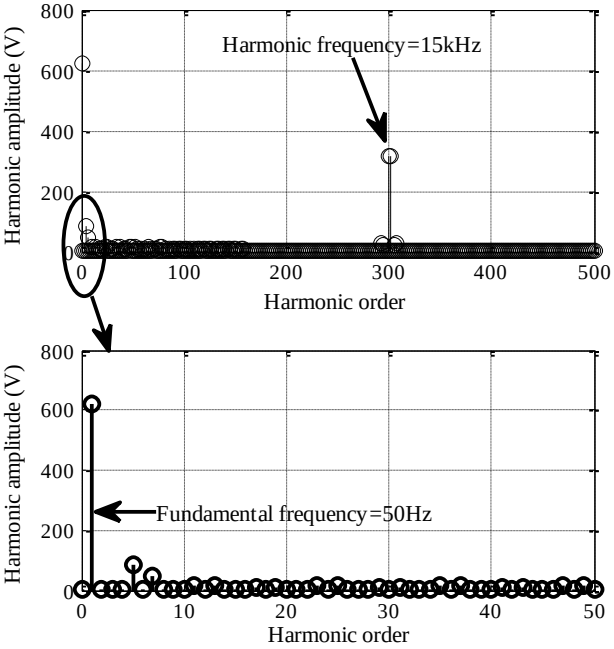

Fig.9 Harmonic content in line voltage for a reference voltage of 0.85 pu.

III. ANALYSIS OF SOFT SWITCHING SVPWM INVERTER

The schematic 3-level 3-phase voltage source soft switching inverter circuit is shown in Fig.10. This circuit has two identical Auxiliary Active Resonant DC Link (ARDCL) snubbers connected to the high voltage DC busline.

The main circuit, ARDCL-1 circuit acts at the transition between state-A and state-B. On other hand, ARDCL-2

circuit acts at the transition between state-B and state-C. The commutation principle from state B to state A is briefly under a condition of ideal switching power semiconductor devices; assume the load current is kept constant during soft switching period.

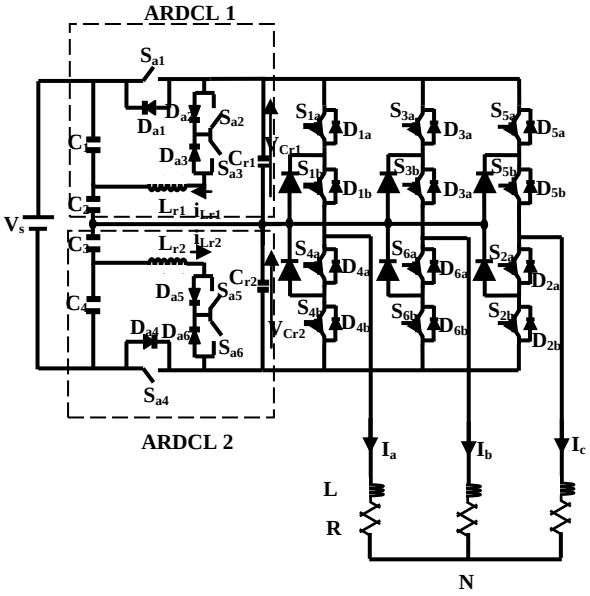

Fig.10 3-level 3-phase soft switching voltage source inverter.

The operation principle of this inverter is described as follows [11]

State-B: mode-1 [t_0, t_1]:

During this mode shown in Fig. 11,the load current I_x is flowing through the main switch S_{1b}, while S_{1b} and S_{4a} are on, the auxiliary switch S_{a1} is on.

State-B: mode-2 [t_1, t_2]:

In this mode, shown in Fig. 12, the auxiliary active power switch S_{a3} is turned-on, thus the resonant inductor current i_{Lr1} flowing through D_{a2} and S_{a3} starts increasing**.** This mode ends when the resonant inductor current i_{Lr1} reaches I_x+I_{b1}, where I_{b1}; the first boost current.

State-B: mode-3 [t_2, t_3]:

During this mode S_{a1} is turned-off, the resonant capacitor C_{r1} starts discharge resonantly. This operation is based on a quasi-resonance owing to L_{r1} and C_{r1} as shown in Fig. 13.

State-B: mode-4 [t_3, t_4]:

When the resonant capacitor voltage V_{Cr1} reach zero, D_{1a} starts conducting as shown in Fig. 14 and i_{Lr1} starts to decrease linearly**.** This mode ends when the resonant inductor current i_{Lr1} decreases to zero.

State-B: mode-5 [t_4, t_5]:

In this mode shown in Fig. 15**,** i_{Lr1} and V_{Cr1} are zero. This mode is called (zero voltage holding mode) and S_{a3} is turned-off.

State-B: mode-6 [t_5, t_6]:

During this mode shown in Fig. 16, the auxiliary switch S_{a2} is turned-on and i_{Lr1} starts increasing linearly towards negative direction**.** This mode ends when the resonant inductor current i_{Lr1} reaches $-I_{b2}$, where $-I_{b2}$; the second boost current.

State-B: mode-7 [t_6, t_7]:

During this mode shown in Fig. 17, the active power switch S_{4a} is turned-off, the resonant capacitor voltage V_{Cr1} starts charging to Vs/2

State-B: mode-8 [t_7, t_8]:

In this mode shown in Fig. 18, Da1 starts to conduct and i_{Lr1} decreases linearly towards negative direction. This mode ends when the resonant inductor current i_{Lr1} reaches zero.

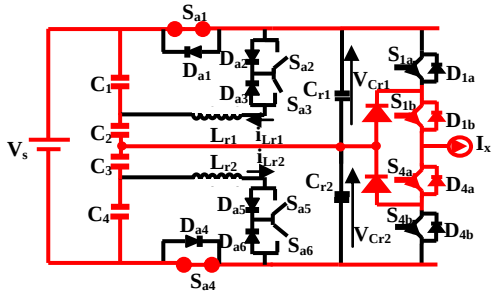

Fig.11 State-B: mode-1 operation trajectory.

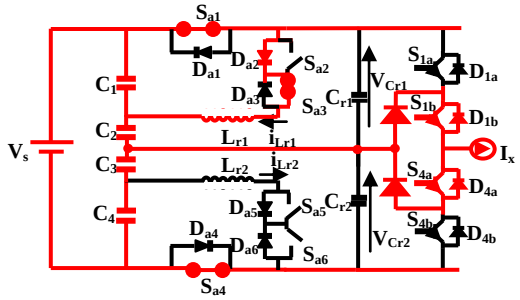

Fig.12 State-B: mode-2 operation trajectory.

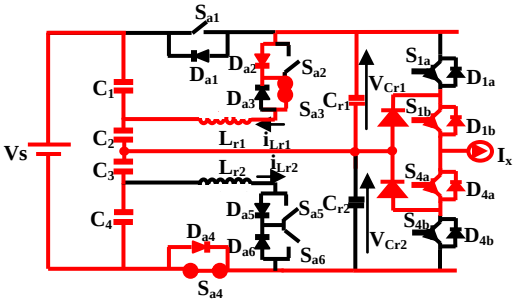

Fig.13 State-B: mode-3 operation trajectory.

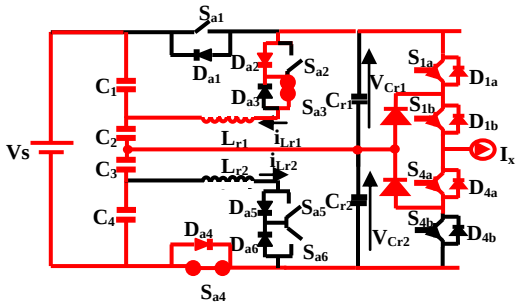

Fig.14 State-B: mode-4 operation trajectory.

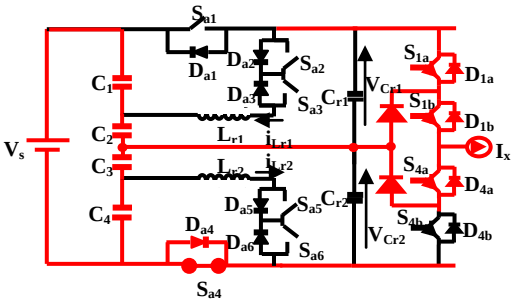

Fig.15 State-B: mode-5 operation trajectory.

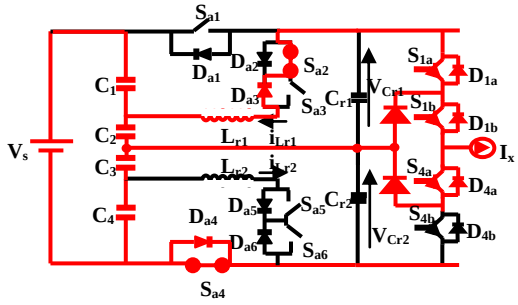

Fig.16 State-B: mode-6 operation trajectory.

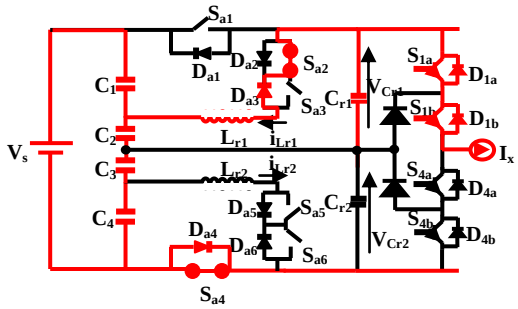

Fig.17 State-B: mode-7 operation trajectory.

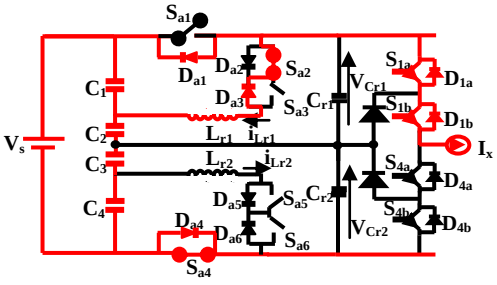

Fig.18 State-B: mode-8 operation trajectory.

The design specifications of these modes are Vs=1000 V, I_x=20 A, L_{r1}=100 μH, r_{Lr1}=0.2 Ω, C_{r1}=0.141 μF, F_s is sampling frequency=15 kHz.

The commutation from state-A to state-B principally has the same modes of operation for transition from state-B to state-A. The theorical waveforms of these modes can be shown in Fig. 19.

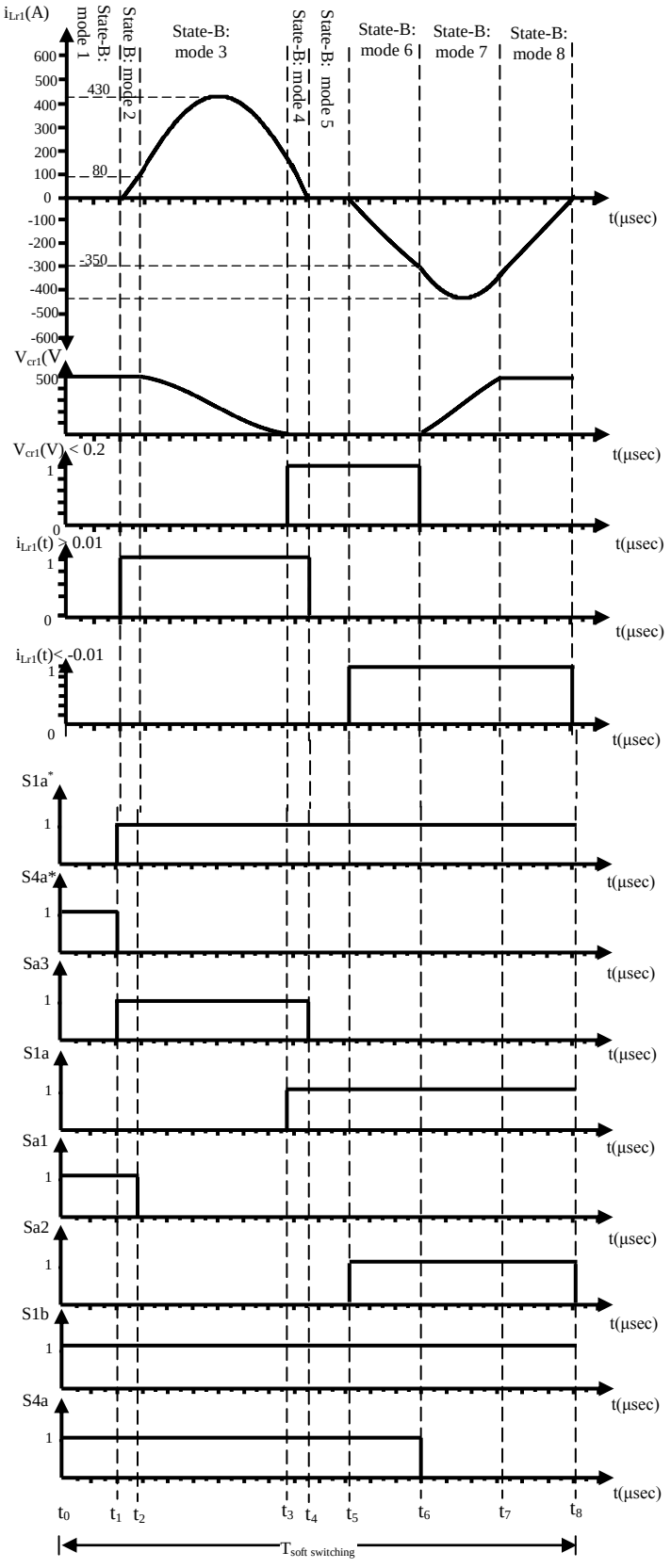

Fig.19 The theorical waveforms of soft switching modes.

IV. SIMULATION VERIFCATION

Simulation has been carried out using MATLAB software to verify the effectiveness of the proposed circuit. Figure 20 shows the proposed software of the soft-switching inverter with the auxiliary resonant circuit. The soft-switching circuit can be divided into two parts as shown in Fig. 21. The first part (circuit 1) acts for transition form state-A to state-B while second part (circuit 2) acts for transition from state-B to state-C and vice versa. Circuit 1 is divided into six blocks as shown in Fig. 22. This circuit acts to generate pulses of auxiliary switches (Sa1, Sa2 and Sa3) and pulses of main switches (S1a, S4a, S3a, S6a, S5a and S2a). Circuit 2 has same construction of the circuit 1, and used to generate pulses of auxiliary switches (Sa4, Sa5 and Sa6) and the pulses of main switches (S1b, S4b, S3b, S6b, S5b and S2b).

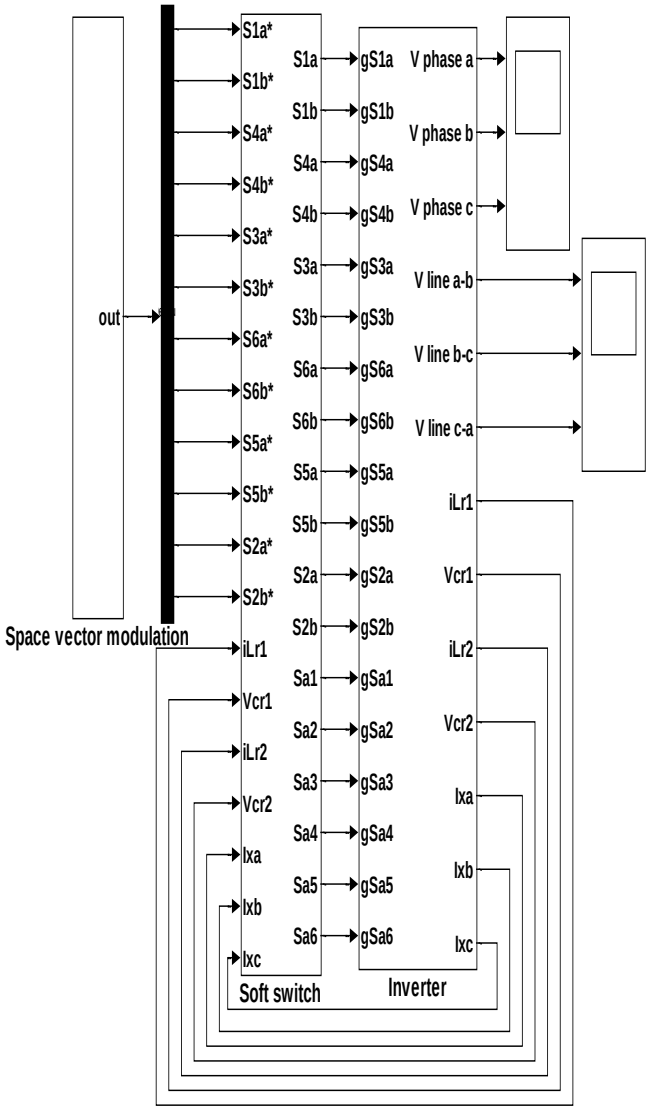

Fig.20 Block diagram of proposed software circuit..

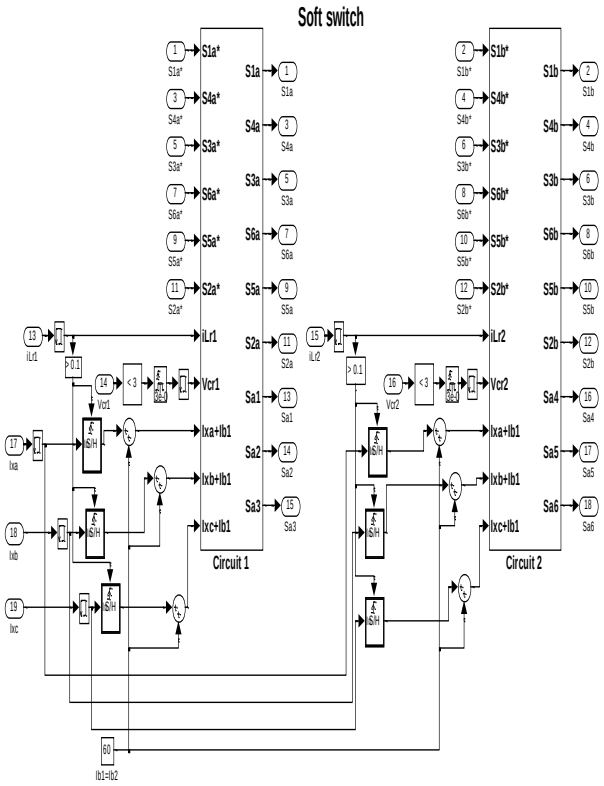

Fig.21 Proposed soft-switching circuit.

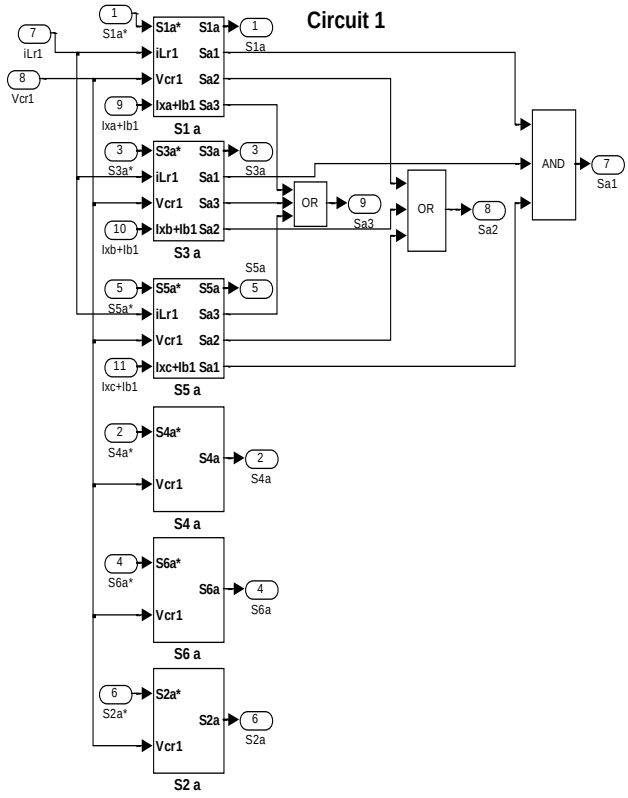

Fig.22 Proposed circuit of transition from state-B to state- A

V. SIMULATION RESULT

For simulation studies, the variation of the phase voltage THD with switching frequency (fs) at several values of modulation index (m) for two loads (resistive and inductive loads) are shown in Figs. 23 and 24. These figures show that the minimum value of THD occurs near switching frequency of 15 kHz.

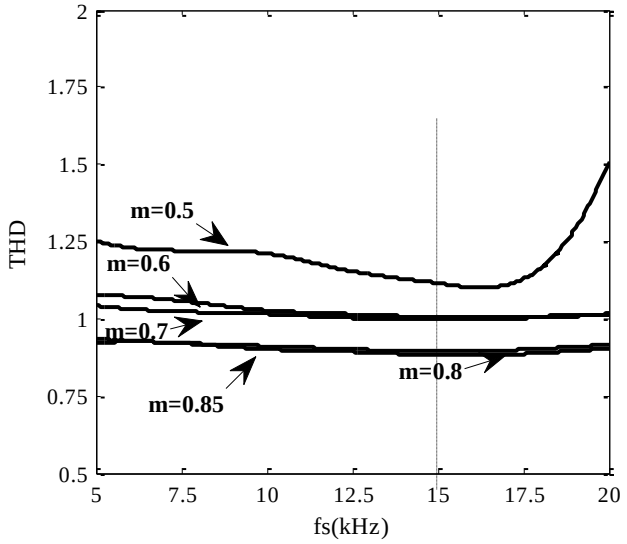

Fig.23 THD against fs for several modulation indexes at resistive load.

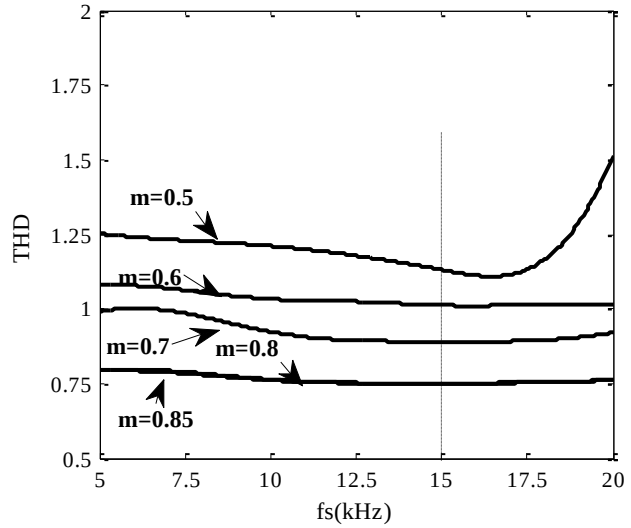

Fig.24 THD against fs for several modulation indexes at inductive load.

It is important to compare the total power losses with modulation index for both hard and soft circuits. The losses in the soft circuit are less than the hard circuit and minimum losses occur at modulation index equal to 0.7. This result is shown in Fig. 25.

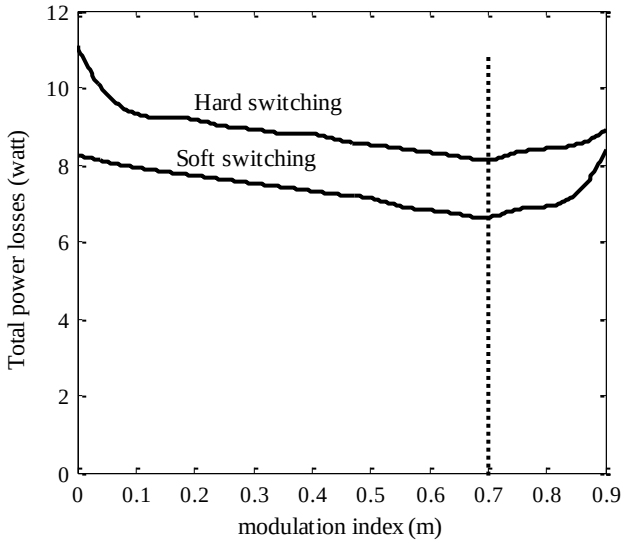

Fig.25 Total power losses versus modulation index for hard and soft –switching.

Figures 26 and 27 show the simulation results for the phase output voltages, and line output voltages, respectively at a modulation index m=0.7, fundamental frequency f=50 Hz and Sampled frequency fs=15kHz. The load current at inductive load is shown in Fig.28. The harmonic content of output voltage is shown in Fig.29. This figure proves the ability of the used SVPWM to produce an output voltage with almost negligible low order harmonics.

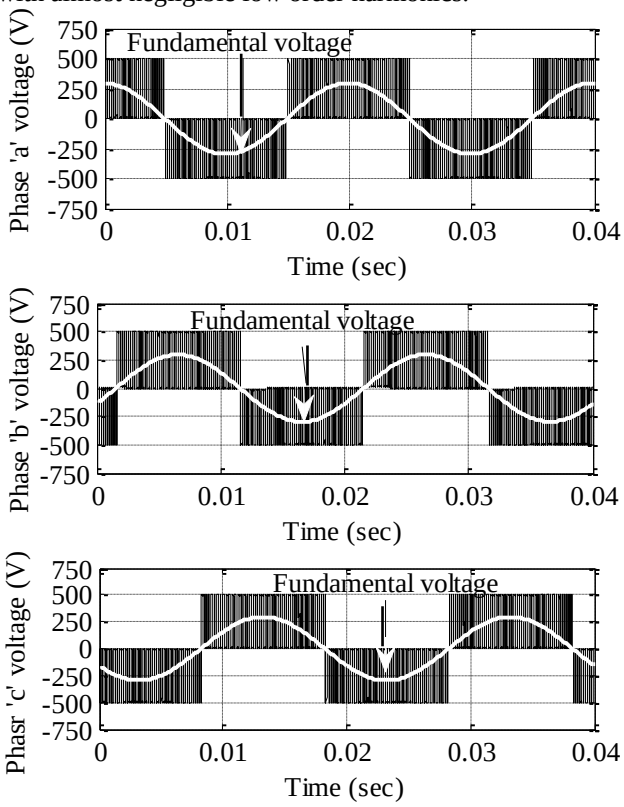

Fig.26 Inverter with soft-switching phase voltages for a modulation index of 0.7 pu.

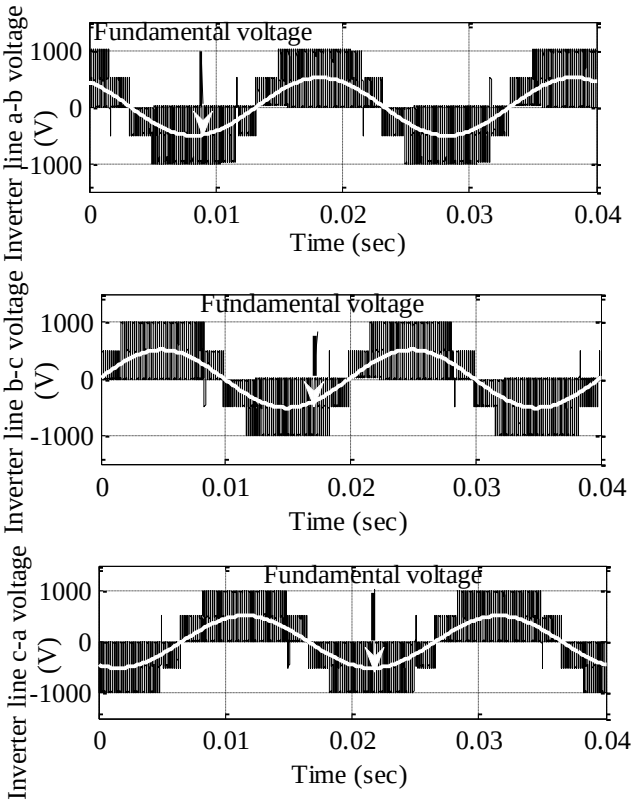

Fig.27 Inverter with soft-switching line voltages for a modulation index of 0.7 pu.

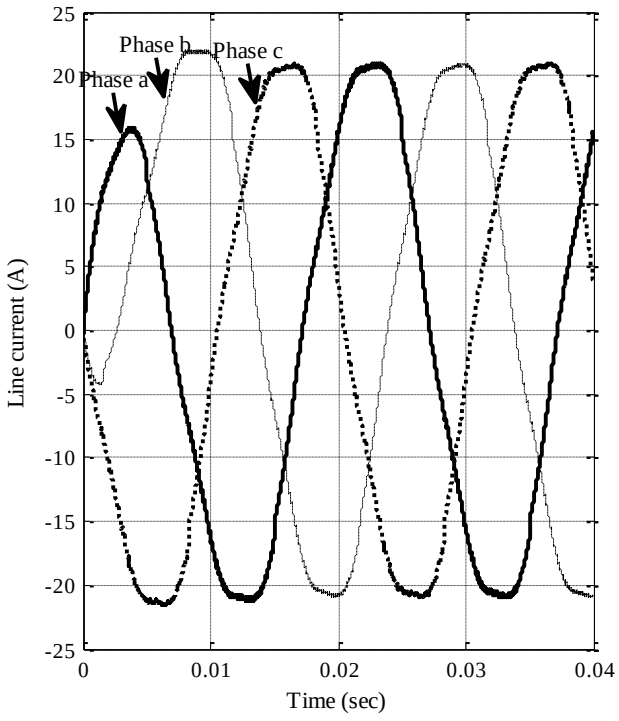

Fig.28 Inverter line currents for inductive load a modulation index of 0.7 pu.

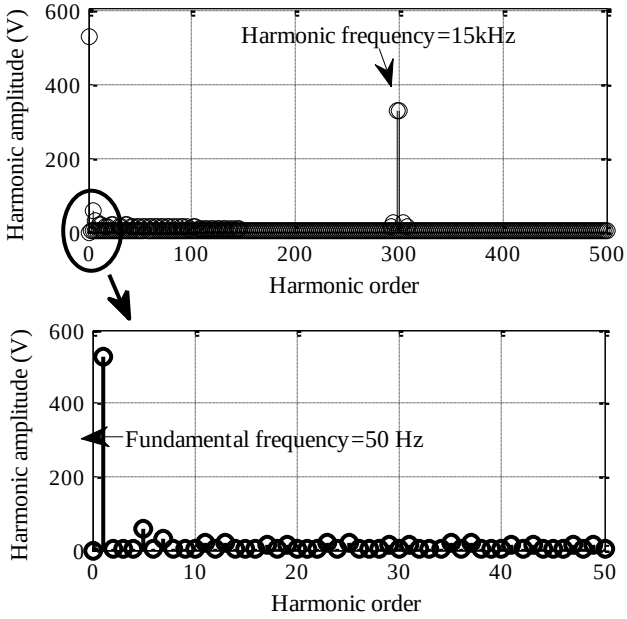

Fig.29 Harmonic content in line voltage for a reference voltage of modulation index of 0.7 pu.

The total losses are almost independent on frequency; this is shown in Fig. 30. The variations of the RMS value of phase voltage and the fundamental phase voltage with modulation index are shown in Figs. 30 and 31.

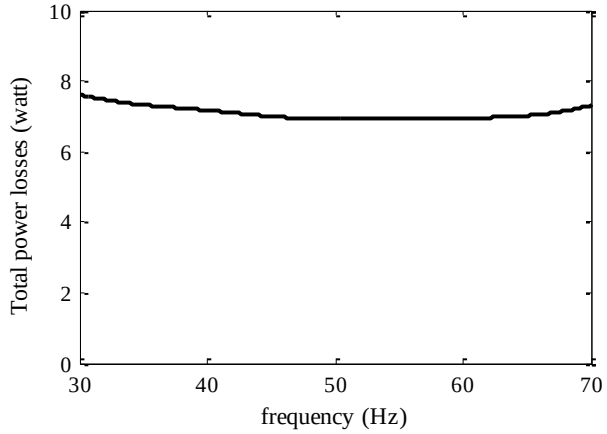

Fig.30 Total power losses versus frequency.

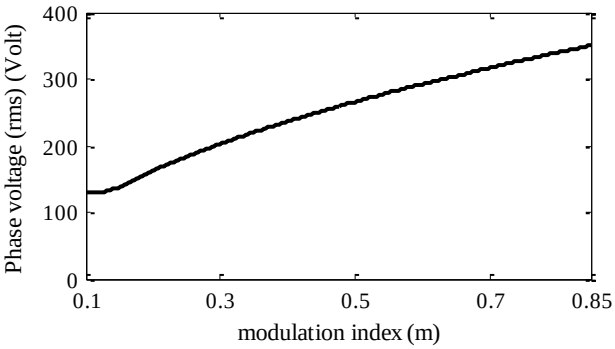

Fig.31 Phase voltage versus modulation index.

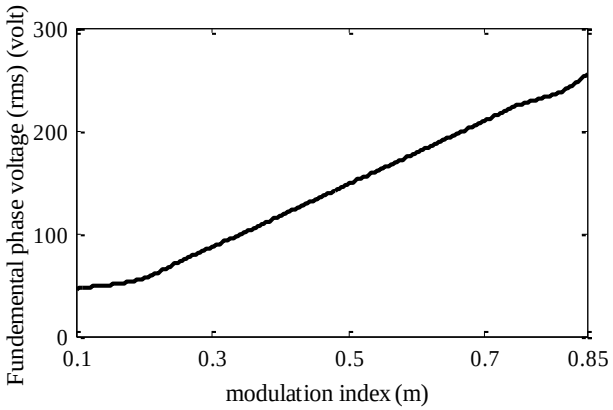

Fig.32 Fundamental phase voltage versus modulation index.

The simulation results that prove the ability of the proposed control circuit to accomplish soft switching process are shown in Figs. 33 and 34. These figures show the ZVS of the main inverter switches in phase (a) and (b) respectively.

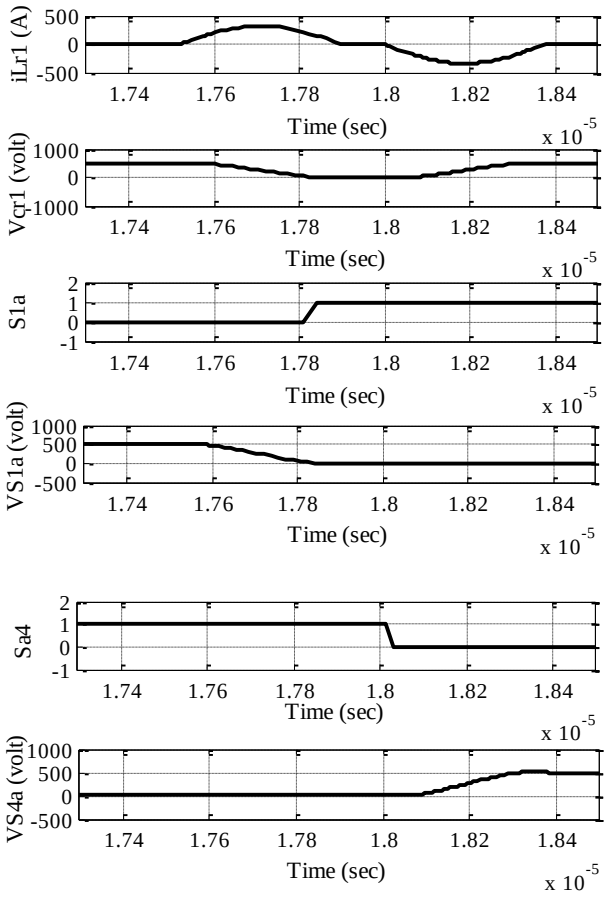

Fig.33 The ZVS waveforms of the main inverter switches in phase a.

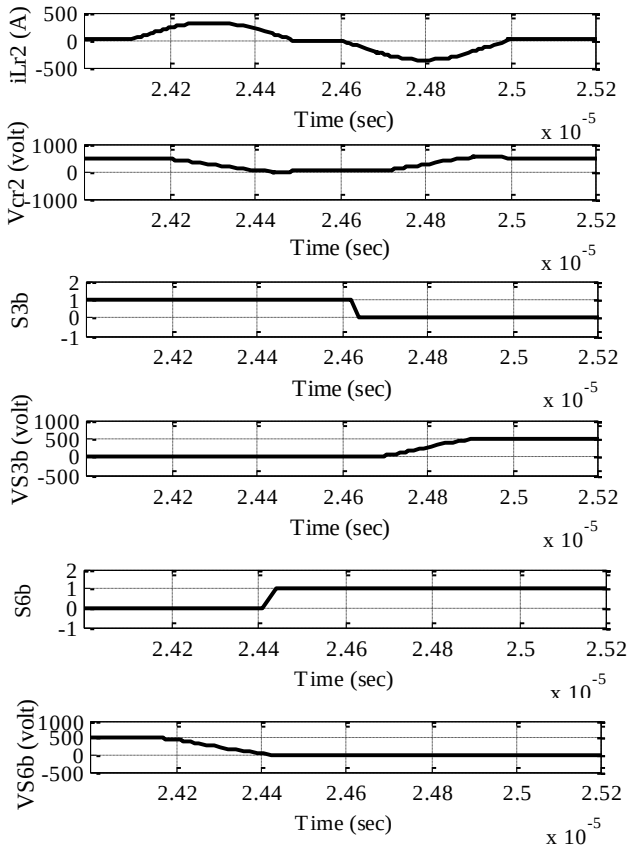

Fig.34 The ZVS waveforms of the main inverter switches in phase b.

Figures 35 and 36 show the voltage across the main switch and the current through it in the same switching period. The voltage and current overlap here is considerably smaller in case turned on and off. This means that the switching losses are considerably reduced.

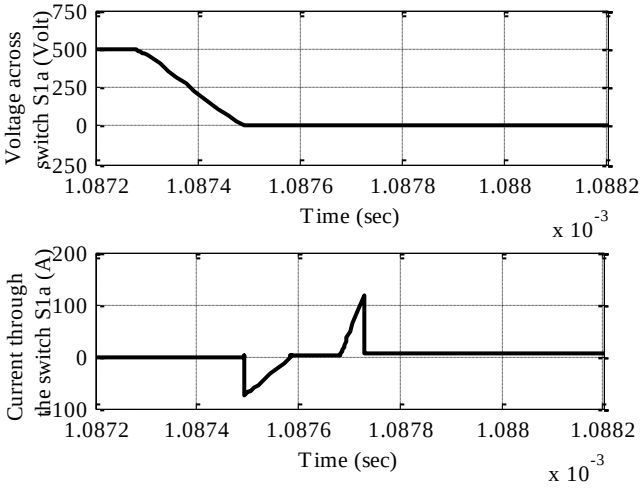

Fig.35 The waveforms of the voltage and the current of the main inverter switches in phase a at turn-on with ZVS.

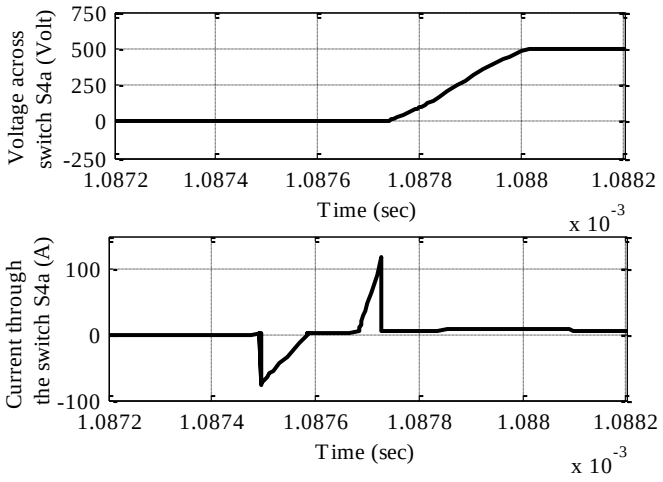

Fig.36 The waveforms of the voltage and the current of the main inverter switches in phase a at turn-off with ZVS.

VI. Conclusion

This paper has presented the steady-state operation principle of the three-level three-phase voltage source inverter with two identical Auxiliary Active Resonant DC Link (ARDCL) snubbers connected to the high voltage DC bus line. The auxiliary circuits are activated during the transition of main switches. The main switches are turned-on and off at zero-voltage condition. It is possible to present the superiority in total power loss characteristic of soft switching inverter from that of hard switching inverter. Simulation results are provided to support the effectiveness of the proposed soft-switching three-phase inverter. Successful operation of this circuit was demonstrated in simulation implementation.

References

[1] J.Lai, F.Peng, "Multilevel Converter-A New Breed of Power Converters", IEEE Transactions on Industry Application, Vol. 32, No.3, pp. 509-517, May/June 1996.

[2] A.K.Guptaand A.M.Khambadkone, "A Space Vector PWM Scheme for Multilevel Inverter Based on Two-level Space Vector PWM", IEEE Trans. Ind. Electronic, Vol.53, No.5, pp.1631-1639, Oct.2006.

[3] R.Teodorescu, F.Blaubjery, J.K.Pedersen, E.Cengelcj and P.N.Enjeti " Multilevel Inverter by Cascading Industrial VSI" IEEE Trans. on Ind. Electron., Vol.49,No.4,pp. 832-838,Aug.2002.

[4] L.M.Tolbert, F.Z.Peng and T.G.Habetler "Multilevel PWM Methods at Low Modulation Indices" IEEE Trans. on Power Electron.,Vol.15,No.4,pp.719-725,July.2000.

[5] A.R.Beig, G.Narayanan and V.T.Ranganathan "Modified SVPWM Algorithm for Three Level VSI with synchronized and symmetrical waveforms" IEEE Trans. on Ind. Electron.,Vol.54,No.1,pp.486-494,Feb.2007.

[6] W. Yu, J. Lai and S.Y. Park " An Improved Zero-Voltage Switching Inverter Using Two Coupled Magnetic in One Resonant Pole" " IEEE Trans. on Power Electron.,Vol.25,No.4,pp.952-961,April.2010.

[7] R. Huang and S. K. Mazumder "A Soft Switching Scheme for Multiphase DC/Pulsating-DC Converter for Three-Phase High-Frequency-Link Pulse width Modulation (PWM) Inverter" IEEE Trans. on Power Electron.,Vol.25,No.7,pp.1761-1774,July.2010.

[8] H. Zhang, Q. Wang, E. Chu, Xi. Liu, and L. Hou "Analysis and Implementation of A Passive Lossless Soft-Switching Snubber for PWM Inverters" IEEE Trans. on Power Electron. Vol. 26, No.2, pp. 411-426,Feb.2011.

[9] P.S.Kumar, J.Amarnath and S.V.L.Narasimham,"An Effective Space-Vector PWM Method for Multilevel Inverter Based on Two-Level Inverter" International Journal of Computer and Electrical Engineering,Vol.2,No.2,pp.243-250, April,2010.

[10] Rabee' H. Thejel "Fuzzy Logic Based Speed Control of a Multiphase Series- Connected Multimotor Drive System Fed from SVPWM VSI" PhD. Thesis, Basrah University, pp.67-69,July.2008.

[11] M.Yamamoto, H. Iwamoto, E.Hiraki,, T.Horiuchi, Y.Sugawara and M.Nakaoka "3- level 3-phase Voltage Fed Soft Switching Inverter with New Space Voltage Vector Modulation Scheme and Its Feasible Evaluations" Power Electronics and Variable Speed Drive,, Yamaguchi university, Yamaguchi,Japan,pp.541-547,18-19 September 2000.